ABSTRACT OF THE DISCLOSURE

A ferroelectric memory has a memory cell array of memory cells having ferroelectric capacitors, which is divided into a plurality of blocks, a boost power circuit provided in each block of the memory cell array to generate a boost voltage required for operation of the memory, a boost power switch provided between a power line connected to an external power terminal and a power supply terminal of each boost power circuit, and remaining ON during normal operation of the memory, a voltage detector circuit for detecting a drop of voltage level of the power line, and a switch control circuit for turning off the boost power switches in the blocks of the memory cell array excluding the boost power switch in a currently selected block in response to the voltage detector circuit.